IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 6, 7, and 11 and CANCEL claims 12-14 in accordance with the following:

1. (CURRENTLY AMENDED) An apparatus for branch prediction, comprising:

a history register storing history of previous branch instructions;

an index generation circuit generating a first index from an instruction address and the history stored in said history register;

a history table storing a tag, which is a predetermined portion of the instruction address, and a first count value indicative of a likelihood of branching in association with the first index, said history table indicating a hit in response to a match between the tag and the predetermined portion of a current instruction address, and indicating a miss in response to a mismatch between the tag and the predetermined portion of the current instruction address;

a branch destination buffer storing a branch destination address or a predicted branch destination address of an instruction indicated by the instruction address and a second value indicative of a likelihood of branching in association with a second index that is at least a portion of the instruction address; and

a selection unit making a branch prediction by selecting one of the first value and the second value depending on whether said history table indicates a hit or a miss.

2. (ORIGINAL) The apparatus as claimed in claim 1, wherein said selection unit selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has an entry therein corresponding to the current instruction address and current history, and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history.

3. (PREVIOUSLY PRESENTED) The apparatus as claimed in claim 2, wherein said

selection unit makes the branch prediction indicating no branching if said branch destination buffer does not have an entry therein corresponding to the current instruction address.

4. (ORIGINAL) The apparatus as claimed in claim 1, wherein said index generation circuit generates the first index that is an Exclusive-OR between the history stored in said history register and the current instruction address.

5. (ORIGINAL) The apparatus as claimed in claim 1, wherein more than one said history table is provided so as to allow a plurality of entries to be registered with respect to said first index.

6. (CURRENTLY AMENDED) A processor, comprising:

a history register storing history of previous branch instructions;

an index generation circuit generating a first index from an instruction address and the history stored in said history register;

a history table storing a tag, which is a predetermined portion of the instruction address, and a first count value indicative of a likelihood of branching in association with the first index, said history table indicating a hit in response to a match between the tag and the predetermined portion of a current instruction address, and indicating a miss in response to a mismatch between the tag and the predetermined portion of the current instruction address;

a branch destination buffer storing a branch destination address of an instruction indicated by the instruction address and a second value indicative of a likelihood of branching in association with a second index that is at least a portion of the instruction address;

a selection unit making a branch prediction by selecting one of the first value and the second value, depending on whether said history table indicates a hit or a miss;

an execution control unit controlling execution of instructions; and

an execution operation unit executing the instructions.

7. (CURRENTLY AMENDED) A method of branch prediction, comprising:

storing a tag, which is a predetermined portion of an instruction address, and a first count value indicative of a likelihood of branching in association with a first index that is generated from the instruction address and history of a previous branch instruction, a hit being indicated in response to a match between the tag and the predetermined portion of a current instruction address, and a miss being indicated in response to a mismatch between the tag and

the predetermined portion of the current instruction address;

storing a branch destination address in a branch destination buffer of an instruction indicated by the instruction address and a second value indicative of a likelihood of branching in association with a second index that is at least a portion of the instruction address;

selecting one of a first value and a second value depending on whether a hit or a miss is indicated; and

predicting branching in response to the selected one of the first value and the second value.

8. (PREVIOUSLY PRESENTED) The method as claimed in claim 7, wherein said selecting one of the first value and the second value selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has an entry therein corresponding to the current instruction address and current history, and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history.

9. (PREVIOUSLY PRESENTED) The method as claimed in claim 8, further comprising:

registering the current instruction address in said branch destination buffer if said branch destination buffer does not have an entry therein corresponding to the current instruction address; and

registering information about the current instruction address in the history table if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history and if a prediction made based on the second value turns out to be erroneous.

10. (ORIGINAL) The method as claimed in claim 9, wherein the information about the current instruction address is not registered in said history table if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history and if the prediction made based on the second value turns out to be correct.

11. (CURRENTLY AMENDED) An apparatus for branch prediction, comprising:

a history register storing history of immediately preceding branch instructions;

an index generation circuit generating a first index that is an Exclusive-OR between an instruction address and the history stored in said history register;

a history table storing a tag, which is a predetermined portion of the instruction address, and a first count value indicative of a likelihood of branching in association with said first index, said history table indicating a hit in response to a match between the tag and the predetermined portion of a current instruction address, and indicating a miss in response to a mismatch between the tag and the predetermined portion of the current instruction address;

a branch destination buffer storing the portion of the instruction address as the tag, a branch destination address of an instruction indicated by the instruction address, and a second value indicative of a likelihood of branching in association with said second index that is a portion of the instruction address; and

a selection unit making a branch prediction by selecting one of the first value and the second value, depending on whether said history table indicates a hit or a miss, wherein said selection unit selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has an entry therein corresponding to the current instruction address and current history, and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history.

12. (CANCELLED)

13. (CANCELLED)

14. (CANCELLED)